layers of the laminated body, and winding directions of adjacent ones of the at least four inductors are opposite to each other.

5. The delay line according to claim 8, wherein one of the plurality of capacitors is connected to an end of at least one of the at least four inductors, and another of the plurality of capacitors is connected to another end of said at least one of the at least four inductors, are located at different positions in a laminating direction of the insulating layers.

6. A delay line comprising:

a coil divided into at least three inductors; and

a laminated body including a plurality of insulating layers and at least three stages of low pass filters including said at least three inductors and a plurality of capacitors; wherein

the at least three inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body; and

a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

8. A delay line comprising:

a coil divided into at least four inductors; and

a laminated body including a plurality of insulating layers and at least four stages of low pass filters including said at least four inductors and a plurality of capacitors.

10. The delay line according to claim 2, wherein the insulating layers have a plurality of via holes for connecting the coil conductor patterns that define the at least four inductors.

13. The delay line according to claim 8, wherein the insulating layers include magnetic material.

20. A monolithic circuit array including a delay line comprising:

a coil divided into at least three lumped constant inductors; and

a plurality of insulating layers stacked on each other to define a monolithic laminated body, the laminated body including at least three stages of low pass filters defined by said at least three lumped constant inductors and a plurality of capacitors; wherein

the at least three lumped constant inductors are defined by a plurality of coil conductor patterns arranged on the same plane of the insulating layers of the laminated body; and

a ratio of a vertical dimension to a lateral dimension of each of the coil conductor patterns is approximately 1.

22. The monolithic circuit array according to claim 20, wherein the number of the plurality of capacitors is greater than the number of the lumped constant inductors.